DCEL301

Reg. No. | | | | | | | | |

III Semester B.Sc. Degree Examination, April - 2023

ELECTRONICS-III

Programming in 'C' and Digital Design Using Verilog

Paper : ELE - CT - 3

(NEP - 2020 Scheme)

Time : 2½ Hours **Maximum Marks : 60**

Instructions to candidates:

i) Answer all questions from part A, any Four questions from Part -B and any four question from Part-C.

Note: ii)s Answer all the question of Part -A in any one page and to be answered only one in this page, answering the same question multiple times will not be answered for evaluation.

PART - A

Answer all the subdivisions. **(12×1=12)**

1. i. Standard ANSI C recognizes _____ number of keywords
   a) 30 b) 32
   c) 24 d) 36

   ii. Which one of the following is not a valid identifier
   a) _alphanumeric b) 1 alphanumeric
   c) alpha_numeric d) alphanumeric 1

   iii. Maximum number of elements in the array declaration int[6] [4] is
   a) 26 b) 24
   c) 36 d) 16

   iv. A function which calls itself is called a _function.
   a) Self function b) Auto Function
   c) Recursive Function d) Static Function

   v. What is the abbreviation of C STDIO in stdio.h.?
   a) Standard Input Output b) Store Input Output
   c) String Terminating Operations I/O d) None of the above

   vi. What is the output of Bitwise OR operation/ on (0110 /1100).?
   a) 1110 b) 1100
   c) 1000 d) 1010

   vii. Which is legal negative number in verilog
   a) 6'd-3 b) 6'-d3
   c) -6'd3 d) None

[P.T.O.

viii. What is the default value for reg data type

a) 1 b) 0

c) X d) Z

ix. Which model uses transistors as their basic components?

a) Switch model b) Gate level

c) Circuit level d) Layout model

x. <= is used in

a) Blocking b) Non-blocking

c) Both d) None

xi. @posedge means

a) Transition from x to 1 b) Transition from 0 to 1, x or z

c) Transition from z to 1, x c) None of these

xii. In continuous assignment statement LHS can be

a) Scalar net b) Vector net

c) Concatenation of both d) all of the above

PART - B

Answer any FOUR questions. **(4×7=28)**

2. What is variable? Explain primary data types used in C programming.
3. What do you mean by looping? Describe any two looping statements in 'C' programming with examples.
4. Describe different Relational, Logical, Bitwise and Arithmetic operators available in C programming language.
5. Explain the following descriptive styles of system hardware with the verilog HDL with example. i) Structural description. ii) Behavioral description.
6. i) Differentiate between Verilog and VHDL
   ii) Differentiate between net and reg
7. Explain arithmetic and logical operators with examples in verilog HDL.

PART - C

Answer any FOUR questions. **(4×5=20)**

8. Write a program in C to generate Fibonacci series up to n elements.
9. Write a C program to read and find largest number among given three numbers.
10. Write a program in C to find roots of quadratic equation.
11. Write a verilog module to realize half subtractor in dataflow description.
12. Write a binary to gray converter module using behavioral description.
13. Write a verilog module to realize the truth table of basic logic gate.