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IV Semester B.Sc. Examination, May/June - 2019

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ELECTRONICS - IV

Digital Electronics and Verilog

(CBCS)(F+R) (2015-16 & Onwards)

Time : 3 Hours | Max. Marks : 70

Instructions : *(1) Answer **all** questions from **Part-A, any five** questions from **Part-B** and **any four** questions from **Part-C**.*

*(2) It is required to answer **all** questions of **Part-A** in **any one** page and to be answered only once. In this Part answering the same question multiple times will not be considered for evaluation.*

PART - A

1. Answer **all** the subdivisions : **15x1=15**

(i) A quantity having continuous values is :
(a) digital (b) analog
(c) a binary (d) all the above

(ii) The output of an AND gate is HIGH when :
(a) any input is HIGH
(b) all inputs are HIGH
(c) None of the inputs are HIGH
(d) both (a) and (b)

(iii) In a certain digital circuit, the time period of the applied signal is twice the pulse width. The duty cycle is :
(a) 100% (b) 200%
(c) 50% (d) 66.66%

(iv) A4-variable Karnaugh Map has :
(a) three cells (b) eight cells
(c) sixteen cells (d) four cells

(v) Block Diagram of half-adder consists of :
(a) two inputs and two outputs
(b) three inputs and two outputs
(c) two inputs and three outputs
(d) two inputs and one output

(vi) In a 4-bit binary weighted resistor type D/A converter most significant bit resistor is 10 kΩ. The least significant bit resistor used is :
(a) 1.25 kΩ (b) 12.5 kΩ (c) 40 kΩ (d) 80 kΩ

(vii) A JK flip-flop is in toggle state when :
(a) J=1, K=0 (b) J=1, K=1
(c) J=0, K=0 (d) J=0, K=1

(viii) The content of a 4-bit register is 1001. The register is shifted 3 times to the left. The content of the register will be :
(a) 1000 (b) 0011 (c) 0110 (d) 1001

P.T.O.

(ix) Register is a :
(a) Set of instructions in a digital computer
(b) Set of paper tapes and cards put in a file
(c) Sequential circuit
(d) None of the above

(x) In order to build a mod-14 down counter the minimum number of flip flops required are :
(a) 5 (b) 2 (c) 4 (d) 3

(xi) Which module is available in Verilog but not in VDHL ?
(a) Behavioral level (b) Switch level
(c) Gate level (d) Data flow level

(xii) Which logic level is **not** supported by Verilog ?
(a) F (b) X (c) Z (d) 1

(xiii) In Verilog the identifier beginning with _____ character is interpreted as a system task or as system function.
(a) # (b) // (c) $ (d) ^

(xiv) In Verilog 'h2A3' is a :
(a) 16-bit Hex number (b) 32-bit Hex number
(c) 4-bit Hex number (d) 8-bit Hex number

(xv) If time scale is defined as timescale 10ns/1ns and #1.75 a=b; then 'a' gets 'b' after
(a) 10 ns (b) 11 ns (c) 17.5 ns (d) 18 ns

PART - B

Answer **any five** questions. **5x7=35**

2. Verify the universal property of NOR gate by realizing AND, OR, NAND and XNOR gates. 7

3. (a) What is Full-adder ? Draw the circuit diagram using logic gates and write its truth table. 4
(b) What is a demultiplexer ? Draw the logic diagram of 1 : 4 demultiplexer. 3

4. (a) With a circuit diagram, explain the working of 4-bit binary weighted D to A converter. 5
(b) Differentiate between combinational and sequential logic circuits. 2

5. Explain the working of clocked RS flip-flop with circuit diagram using only NAND gate. Draw the truth table and timing diagram. 7

6. What is a shift register ? Draw the logic diagram of a 4-bit serial-in serial-out shift register. Explain how the data 1010 is written and retrieved. Also draw the timing diagram. 7

7. (a) Compare VHDL and Verilog. 5+2
   (b) Write the basic module of Verilog Programming.

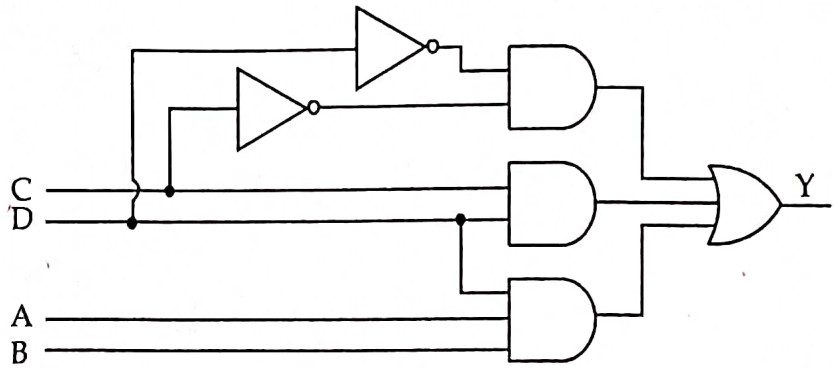
8. Explain Logical and Reduction operators in Verilog with examples. 7

9. Explain initial and always statements in behavioral modeling. 7

PART - C

Answer **any four** questions. **4x5=20**

10. Write the Boolean expression for the output Y in the given logic diagram by mentioning the output at the end of each gate and simplify it using Boolean Laws. 5



11. Simplify the Boolean function $f(A, B, C, D) = \Sigma m(1, 3, 5, 8, 9, 11, 15) + \Sigma d(0, 2, 13)$ Using K-map and realize the simplified expression using basic gates. 5

12. A 4-bit Digital to Analog Converter has a step size of 0.20 V. Determine output voltage for input of 1101 if reference voltage is 5 V and also calculate percentage of resoluton. 5

13. Design a synchronous mod-3 counter using K-map technique. 5

14. Write a Verilog code for binary to gray code and vice-versa. 5

15. Write a Verilog code for 4 : 1 Multiplexer. 5

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