SE – 205

IV Semester B.Sc. Examination, September 2020
(CBCS) (F + R) (2015-16 & Onwards)
ELECTRONICS – IV
Digital Electronics and Verilog

Time : 3 Hours Max. Marks : 70

Instruction: *Answer **all** questions from Part **A**, **any five** questions from Part **B** and **any four** questions from Part **C**.*

Note : *It is required to answer **all** the questions of Part **A** in **any one** page. Answering the same questions multiple times will **not** be considered for evaluation.*

PART – A

Answer **all** the subdivisions. **(15×1=15)**

1. i) The output of an AND gate is LOW
   a) when any input is HIGH
   b) all the time
   c) when all inputs are HIGH
   d) when any input is LOW

   ii) Which of the following is not a valid law of a Boolean algebra ?
   a) $A + 0 = A$ b) $A = A.1$ c) $A.0 = 0$ d) $A + A = 1$

   iii) If a 3-input XOR gate has eight input combinations, then how many combinations result in a HIGH output ?
   a) 1 b) 4 c) 2 d) 8

   iv) If 1 and 0 are the inputs to half adder circuit the result is
   a) Sum-1 Carry-0
   b) Sum-1 Carry-1
   c) Sum-0 Carry-1
   d) Sum-0 Carry-0

   v) In a K-map identify the 3 adjacent min. terms for the min. term X to form a quad.
   a) $\bar{A}\bar{B}\bar{C}\bar{D}$, $A\bar{B}\bar{C}\bar{D}$, $A\bar{B}C\bar{D}$
   b) $A\bar{B}CD$, $ABCD$, $A\bar{B}C\bar{D}$
   c) $A\bar{B}C\bar{D}$, $A\bar{B}\bar{C}D$, $ABCD$
   d) $A\bar{B}\bar{C}D$, $ABCD$, $AB\bar{C}D$

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$				X
$\bar{A}B$				
AB				
$A\bar{B}$				

P.T.O.

vi) Which one of the following can be used as series to parallel convertor ?
a) Decoder
b) Demultiplexer
c) Digital counter
d) Multiplexer

vii) In a 4-bit binary weighted resistor type D/A converter most significant bit resistor is 50 KΩ. The resistor used for the least significant bit is
a) 400 KΩ
b) 100 KΩ
c) 200 KΩ
d) 50 KΩ

viii) A simple flip-flop is
a) is 2 bit memory
b) is 1 bit memory
c) is a four state device
d) has nothing to do with memory

ix) Register is a
a) Set of instructions in a digital computer
b) Set of paper tapes and cards put in a file
c) Temporary storage unit within the CPU
d) Part of the auxiliary memory

x) In order to build a mod-12 counter the minimum number of flip flops required are
a) 2
b) 4
c) 3
d) 1

xi) _____ of the following statements are wrong with respect to Verilog.
a) Keywords are in lowercase
b) Extra white space is ignored
c) Relatively harder to learn
d) Comments may not be nested

xii) _____ level of abstraction level is available in Verilog but not in VHDL.
a) Behavioral level
b) Dataflow level
c) Gate level
d) Switch level

xiii) _____ logic level is not supported by Verilog.
a) F
b) X
c) Z
d) 1

xiv) If A = 4'b0011 and B = 4b'0011, then the result of A**B will be

a) 6 b) 9

c) 27 d) 3

xv) In continuous assignment left hand side must be

a) Net b) Reg

c) Scalar or Vector Net d) Scalar or Vector reg

PART – B

Answer **any five** questions. **(5×7=35)**

2. a) Verify the universal property of NAND gate by realizing AND, OR and NOT gates.

   b) State and prove De-Morgan's theorem. **(4+3)**

3. a) With a circuit diagram explain CMOS inverter.

   b) What is half adder ? Draw the circuit diagram using logic gates and write its truth table. **(3+4)**

4. a) With a relevant circuit diagram, explain the working of 4-bit binary weighted D to A converter.

   b) Draw the logic circuit of 2 : 4 decoder using AND gates. **(5+2)**

5. a) Explain the working of D flip-flop with circuit diagram. Draw the truth table and timing diagram.

   b) Draw the truth table and timing diagram of T flip-flop. **(5+2)**

6. What is a shift register ? Draw the logic diagram of a 4-bit serial-in parallel-out shift register. Explain how the data 1011 is written and retrieved. Also draw the timing diagram. **7**

7. a) Compare VHDL and Verilog.

   b) Write the basic module of Verilog programming. **(5+2)**

8. Explain Arithmetic and logical operators in Verilog with examples. **7**

9. Explain the statements if, if-else and if-elseif-else in Verilog. **7**

PART – C

Answer **any four** questions. **(4×5=20)**

10. Simplify the expression $Y = ABC + \overline{AC} + \overline{A}C(AB + C)$ using Boolean laws and draw the circuit for simplified expressions using basic gates.

11. Simplify the Boolean function f(A, B, C, D) = $\sum$m(1, 3, 5, 8, 9, 11, 15) + d(2, 13) using K-map and realize the simplified expression using basic gates.

12. A 4-bit digital to analog converter has a step size of 0.5 V. Determine full scale output voltage and percentage of resolution.

13. Design a synchronous mod-5 counter using K-map technique.

14. Write a Verilog code for all the logic gates.

15. Write a gate level Verilog code for 4 : 1 multiplexer.