DCEL201

Reg. No. | | | | | | | | |

II Semester B.Sc. Degree Examination, July/August - 2024

ELECTRONICS

Analog and Digital Electronics

(NEP 2020 Scheme)

Paper : ELE-CT2

Time : 2½ Hours **Maximum Marks : 60**

Instructions to Candidates:

Answer **All** the questions from Part-A, any **Four** questions from Part-B and any **Four** questions from Part-C.

Note:

Answer **All** questions of Part-A in any one page, the same questions answered multiple times will not be considered for Evaluation.

PART - A

1. Answer All the subdivisions: **(12×1=12)**

i) In the construction of UJT, emitter contact is

a) Near base 1 b) Exactly in the middle of the channel
c) Near base 2 d) always attached to base 1

ii) Tunnel diode is

a) Heavily doped PN Junction b) Lightly doped PN junction
c) Moderately doped PN Junction d) None of the above

iii) A device that exhibits a negative resistance region is

a) PN junction diode b) UJT
c) Varactor diode d) Solar Cell

iv) The phase shift produced by each RC section in RC phase shift oscillator is

a) 30^0 b) 45^0 c) 90^0 d) 60^0

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v) High pass filters allows

a) low frequency signals b) high frequency signals
c) medium frequency signals d) all signals

vi) Damped oscillations are those whose amplitude _____ with time.

a) Increases b) Remains constant
c) Decreases d) Changes

vii) If 1 and 1 are the inputs to half subtractor circuit the result is

a) Sum -1 and Carry -0 b) Sum -1 and Carry -1
c) Sum -0 and Carry -1 d) Sum -0 and Carry -0

viii) A standard TTL operate with a _____ volt power supply.

a) 2 b) 4 c) 5 d) 3

ix) A 4 variable K map has

a) 8 cells b) 4 cells c) 16 cells d) 32 cells

x) The content of a 4-bit register is 1000. The register is shifted 3 times to the right. The content of the register will be

a) 1001 b) 0011 c) 0001 d) 1000

xi) The minimum number of flip flops required to design mod 5 counter is

a) 5 b) 4 c) 3 d) 2

xii) A JK Flipflop is in toggle state when

a) J=1, K=0 b) J=1, K=1 c) J=0, K=0 d) J=0, K=1

PART - B

Answer any Four questions: **(4×7=28)**

2. a) Draw the symbol of Varactor diode. Mention its applications. **(2+5)**

b) With a circuit diagram. Explain the working of E-MOSFET.

3. a) Draw and explain the working of UJT relaxation oscillator. **(5+2)**

b) Write any two characteristics of an ideal op-amp.

4. a) What is an integrator? Draw the op-amp integrator circuit and sketch the output waveforms for sine and square wave input. **(5+2)**

   b) State the Barkhausen criterion for sustained oscillations.

5. a) Explain: i) Propagation delay ii) Fan-in iii) Fan-out iv) Noise margin. **(5+2)**

   b) Draw the logic diagram of 1:4 demultiplexer.

6. a) Write the truth table and draw the logic diagram using basic gates for Full Adder. **(3+4)**

   b) Explain the working of D Flip flop with circuit diagram. Draw the truth table and timing diagram.

7. a) What is a Shift Register? Explain the working of Serial In Serial Out Shift register with an example. **(5+2)**

   b) Compare synchronous and asynchronous counters.

PART - C

Answer any Four questions: **(4×5=20)**

8. A UJT has $\eta = 0.65$ and $R_{BB} = 8K\Omega$. Calculate

   i) R_{B1} and R_{B2}

   ii) Peak point voltage

   Given V_{BB}=10V and V_D=0.7V.

9. Design the high pass filter with acut off frequency of 2KHz and pass band gain of 5. Given $C = 0.022\mu F$, $R_f = 10K\Omega$

10. A Wien-bridge oscillator has $C = 0.1\mu F$, $R = 4.7K\Omega$ and $R_f = 20K\Omega$. Determine the frequency of oscillations.

11. Draw the truth table and logic circuit for 3:8 decoder.

12. Simplify the Boolean function $f(A, B, C, D) = \Sigma m(1,5,7,8,9,13) + \Sigma d(3,12)$ using K map.

13. Design a synchronous mod -5 counter using K map.